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Goddard Space Flight Center **Greenbelt, MD 20771**	**Approved: 11-21-2019** **Revalidation: 11-21-2024**

Standard Quality Assurance Requirements for Printed Circuit Boards

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NASA GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland 20771

Approved By:

Original Signed By:
Eric Isaac
Director of Safety and
Mission Assurance
Goddard Space Flight Center

Original Signed By:
Felicia Jones
Director of Engineering and
Technology
Goddard Space Flight Center

Original Signed By:
Dave F. Mitchell
Director of Flight Projects
Goddard Space Flight Center

Original Signed by Tupper Hyde For:
Steve Scott
Chief Engineer
Goddard Space Flight Center

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FOREWORD

This standard is published by the Goddard Space Flight Center (GSFC) to provide uniform engineering and technical requirements for processes, procedures, practices, and methods that have been endorsed as standard for NASA GSFC programs and projects, including requirements for design, procurement, quality verifications, and repair of printed circuit boards (PCBs).

This standard establishes requirements that apply to printed circuit boards of all types used for GSFC missions and for engineering model work that directly affects the design or quality of PCBs used in GSFC missions. The requirements address design criteria, procurement instructions, quality requirements, quality data deliverables, and review and approval processes.
Requests for information, corrections, or additions to this standard should be submitted via "Contact GTSP" on the GSFC Technical Standards website at http://standards.gsfc.nasa.gov.

Original Signed by James S. Milne For:
Josef A. Wonsever
Technical Standard Coordinator
Goddard Space Flight Center

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1. SCOPE

1.1 Purpose

The purpose of this standard is to provide requirements and recommendations that ensure that high-reliability printed circuit boards (PCBs) are designed, procured, produced and used in GSFC project mission hardware.

1.2 Applicability

The requirements herein apply across the full lifecycle of PCB design, manufacturing and application. The performance and assurance requirements herein are addressed to organizations who establish PCB requirements, design PCBs, perform PCB design review, procure systems with integrated PCBs, procure PCBs, test or evaluate PCB production lots, assess or certify PCB testing facilities, assure PCBs, and manage risk associated with PCBs that do not meet the requirements herein. Section 6.3 is specific to flowdown of requirements to the PCB vendor.

1.2.1 Flight, Flight Spare and Custom Mission Critical Support Hardware

This Standard defines a standard engineering and quality assurance baseline for all mission risk classes that is applicable to GSFC flight, flight spare and custom mission critical ground support hardware for which spares or lead-time for replacement would be resource-prohibitive and must survive environmental tests. For ground support hardware that must survive environmental testing, it is acceptable to have one or more spares available in lieu of imposing a PCB specification and PCB structural integrity coupon testing if that is more economical than prescribing PCB requirements with PCB structural integrity coupon testing, or if replacement hardware can be readily produced.

Compliance with this Standard can be established for Inherited PCB Designs, Spares, or Build-to-Print Designs, by conducting an inheritance risk assessment in accordance with GPR 8730.5.

1.2.2 Engineering Model Hardware

These requirements shall be applied to engineering model hardware in cases where (1) the engineering model is being used to validate manufacturing processes, (2) the engineering model is going through full environmental testing prior to build of the flight model, or (3) there is a possibility that the engineering model may become a flight spare.

1.2.3 Engineering Development Units

Projects shall limit, or not impose, the requirements stipulated herein to engineering development units so as to enable such units to be produced at a low cost and without expectations for extensive failure analysis. Development units, which are eventually used as flight hardware, are subject to risk assessment. The Project CSO should consult the GSFC Microelectronics Packaging and Printed Circuit Board (MPCB) Commodity Risk Assessment Engineer (CRAE)

for the risk assessment process.

2. APPLICABLE DOCUMENTS

2.1 General

The documents listed in this section contain provisions that constitute requirements of this standard as cited in the text of Sections 4 through 7 , Requirements. The latest issuances of cited documents shall be used. The applicable documents are accessible via the NASA Technical Standards System at http://standards.nasa.gov, directly from the Standards Developing Organizations, or from other document distributors.

2.2 Government Documents

NPR 7120.5	NASA Space Flight Program and Project Management Requirements
GPR 8705.4	Risk Classification Guidelines and Risk-Based SMA Practices for GSFC Payloads and Systems
GPR 8730.5	Safety and Mission Assurance Acceptance of Inherited and Build-to-Print Products
NASA-STD-8739.6	Implementation Requirements for NASA Workmanship Standards
MIL-STD-100	Standard Practice for Engineering Drawings
MIL-PRF-55110	Performance Specification Printed Wiring Board, Rigid, General Specification For
MIL-PRF-31032	Performance Specification Printed Circuit Board/Printed Wiring Board, General Specification For

2.3 Non-Government Documents

Where applicable, the space applications addendum(s) of documents shall apply.

ASTM-E-595	Standard Test Method for Total Mass Loss and Collected Volatile Condensable Materials from Outgassing in a Vacuum Environment
ECSS-Q-ST-70-10C	Qualification of Printed Circuit Boards
ECSS-Q-ST-70-11C	Procurement of Printed Circuit Boards
J-STD-003	Solderability Tests for Printed Boards
IPC-1601	Printed Board Handling and Storage Guidelines
IPC-2221	Generic Standard on Printed Board Design
IPC-2222	Sectional Design Standard for Rigid Organic Printed Boards
IPC-2223	Sectional Design Standard for Flexible Printed Boards
IPC-2225	Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies
IPC-4781	Qualification and Performance Specification of Permanent, Semi-Permanent and Temporary Legend and/or Marking Inks
IPC-6011	Generic Performance Specification for Printed Boards

IPC-6012	Qualification and Performance Specification for Rigid Printed Boards (and Space Addendum)
IPC-6013	Qualification and Performance Specification for Flexible Printed Boards
IPC-6015	Qualification and Performance Specification for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures
IPC-6018	Qualification and Performance Specification for High Frequency (Microwave) Printed Boards (and Space Addendum)
IPC-9252	Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards
IPC-A-600	Acceptability of Printed Boards
IPC-QL-653	Certification of Facilities that Inspect/Test Printed Boards, Components, and Materials
IPC-T-50	Terms and Definitions
IPC-TM-650, Method 2.1.1	Microsectioning, Manual and Semi or Automatic Method
IPC-TM-650, Method 2.4.15	Surface Finish, Metal Foil
IPC-TM-650, Method 2.6.8	Thermal Stress, Plated-Through Holes
IPC-TM-650, Method 2.6.26	DC Current Induced Thermal Cycling Test

2.4 Order of Precedence

1. When this standard is applied as a requirement on a GSFC program or GSFC project, or is imposed by contract or purchase order on a GSFC supplier, the technical requirements of this standard take precedence, in the case of conflict, over the technical requirements cited in the applicable documents in Section 2 herein.
2. When requirements in GSFC project-specific requirement documents, imposed by contract or purchase order on a GSFC supplier, conflict with requirements herein, the requirements of the project-specific document take precedence when approved by the CSO or the Code 300 SMA Technical Authority.
3. When requirements in PCB drawing notes conflict with requirements herein, the PCB drawing notes take precedence over the technical requirements of this standard. See 5.5.
4. Requirements herein that are unique to a certain mission risk class (e.g., Class A, Class B, Class C, Class D) shall be applied in accordance with the mission risk class defined by the project's mission assurance baseline. Requirements herein that are not associated with a particular mission risk class are applicable to all mission risk classes for missions required to follow NPR 7120.5.
5. In the event of a conflict between revisions of the documents described in Sections 2.2 and 2.3 above, the language in the latest revision of a standard shall take precedence.

3. ACRONYMS AND DEFINITIONS

3.1 Acronyms

CAGE	Commercial and Government Entity
Coupon	A portion of quality conformance test circuitry that is used for a specific test, or group of related tests, in order to determine the acceptability of a product.
Coupon strip	Section of the PCB production panel that contains one or more coupon segments

CRAE	Commodity Risk Assessment Engineer
CSO	Chief Safety and Mission Assurance Officer or the designated Project Officer
DID	Data Item Deliverable
ENEPIG	Electroless Nickel Electroless Palladium Immersion Gold
ENIG	Electroless Nickel Immersion Gold
GSFC	Goddard Space Flight Center
IPC	Association Connecting Electronics Industries
ISO	International Organization for Standardization
MEB	Materials Engineering Branch
MPE	Materials and Processes Engineer
MRB	Material Review Board
PCB	Printed Circuit Board
PWA	Printed Wiring Assembly
SEM	Scanning Electron Microscope
SMA	Safety and Mission Assurance
XRF	X-ray Florescence

3.2 Definitions

1. Heritage Hardware, Hardware whose design has been previously qualified and used in space applications, and was accepted for use by a NASA program or project.
2. Inherited Hardware, A piece of hardware or hardware design, brought in to a project, that has some amount of prior history, may be built to different design standards, and may not have had NASA insight into the design or construction.
3. Meta, An integrated information system for process performance, data management and analytics that is operating in support of NASA mission performance, the GSFC Management System and GSFC Supply Chain Risk Management. The system is managed by GSFC's Safety and Mission Assurance Directorate
4. PCB Lot, One or more boards that are traceable to quality testing and inspection performed on representative samples and coupons.
5. Supplier, An organization or company that provides a product or service to the user under a contract.
6. System Developer, An organization or company that provides a subsystem or subsystem related services to the supplier under contract.
7. User , An organization or company that receives products or services from a supplier under a contract.
8. Vendor , An organization or company that offers printed circuit boards or printed circuit board related services.

See IPC-T-50 for technical definitions of PCB-related terms.

4. TRAINING AND CERTIFICATION

PCB designers and inspectors should be capable of performing their job duties in a manner that ensures compliance to the requirements herein. The capability to perform job duties is directly related to training and certification.

4.1 Certification Authority

Applicable PCB designers and inspectors shall be certified by their supervisor or the individual who is responsible for their job assignment as capable of performing to the requirements herein and of continuously meeting the certification criteria in 4.2, 4.3, or 4.4 herein. Evidence of certification that includes the signature of the certification authority and date of certification shall be available for review upon request.

4.2 Personnel Certification - Printed Circuit Board Designers

Personnel who perform printed circuit board layout for boards under this standard shall be certified. The minimum certification criteria for PCB designers are:

4.2.1 IPC Certified Interconnect Designer - Basic (CID) certification or equivalent training/experience

4.2.2 No lapse in designer duties for greater than two years

4.3 Personnel Certification - Printed Circuit Board Inspectors, External Visual

Personnel who perform external visual inspection on PCBs under this standard shall be certified. The minimum certification criteria for PCB inspectors are:

4.3.1 Visual acuity per NASA-STD-8739.6, A.7.6 or IPC-QL-653, 3.5.1.d

4.3.2 IPC-A-600 Certified IPC Specialist (CIS) certification, Modules 1 through 3 or IPC-6012 CIS certification with Space Addendum

4.3.3 No lapse in inspector duties for greater than two years

4.3.4 Equivalent experience can be substituted for formal certification

4.4 Personnel Certification - Printed Circuit Board Inspectors, Microsection

Personnel who perform microsection analysis of PCB test coupons that represent PCBs under this standard shall be certified. The minimum certification criteria for PCB inspectors are:

4.4.1 Visual acuity per NASA-STD-8739.6, A.7.6 or IPC-QL-653, 3.5.1.d

4.4.2 IPC-A-600 Certified IPC Specialist (CIS) certification, Modules 1, 2, and 4 or IPC-6012 CIS certification with Space Addendum

4.4.3 No lapse in inspector duties for greater than two years

4.4.4 Equivalent experience can be substituted for formal certification

5. DESIGN

5.1 Design Standard

5.1.1 PCBs shall be designed in accordance with IPC-2221 (Class 3), Generic Standard on Printed Board Design, and one or more of the following relevant design standards:

1. IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards
2. IPC-2223 Sectional Design Standard for Flexible Printed Boards
3. IPC-2225 Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies

5.1.2 PCB test coupons shall be designed per IPC-2221 into all PCB production panels. See 6.2.3.

5.2 Non-standard Features

Any PCB features that are not defined by the IPC-2220 and IPC-6010 series standards are considered non-standard, and shall be evaluated for possible impacts to hardware performance, reliability, or manufacturing success per 5.5. The evaluation shall be provided to the Project CSO and the GSFC MPCB CRAE to be approved for use prior to final board design.

5.3 Drawings

5.3.1 The PCB drawings shall be used to provide instructions to the PCB vendor related to design intent as well as to flow down applicable quality assurance requirements from this standard.

5.3.2 The design organization shall create a drawing note baseline that addresses all critical requirements.

5.3.3 Direction shall be provided for each applicable requirement characterized by the standards defined in 5.1 and 6.3.3 as "as agreed between the user and the supplier" (AABUS) or requiring specification in the procurement documentation.

5.4 Outgassing Requirements

5.4.1 Nonmetallic materials used in PCB fabrication shall meet acceptance criteria of ≤ 0.1 percent collected volatile condensable materials (CVCM) and ≤ 1.0 percent total mass loss (TML), when tested in accordance with ASTM-E-595.

5.4.2 If outgassing properties of a new material (e.g. laminates, silk screen ink, solder resist, etc.) have not been established, the outgassing properties shall be established. A new material is a material for which there are not pertinent test reports or reports from prior flight history available. The Project materials engineer should decide which tests are applicable. The new material shall be approved by the GSFC Materials Engineering Branch for mission use prior to PCB procurement.

5.5 Design and Process Reviews

5.5.1 PCB Designs for risk classes A and B, PCB master drawings shall be approved by a review team designated by the Project prior to initiation of design or design procurement. This requirement is optional for risk classes, C, D, and Sub-D per GPR 8705.4.

5.5.2 The Review team shall include representatives from the engineering and safety and mission assurance (SMA) directorates, who can represent the interests and perspectives of the technical authorities for PCB design and assurance.

5.5.3 The drawing notes shall be reviewed for compliance with the requirements herein. The complete and approved PCB master drawing shall be included to the lot data acceptance package. Evidence of PCB master drawing approval by the review team shall be provided to the PCB procuring agent.

5.5.4 If the system developer or supplier uses alternate PCB standards for design, manufacturing instructions, or quality test and inspection criteria, these shall be provided to the Project office for review for risk exposure assessment. An alternate standard is defined as a document or a collection of criteria that are different than those contained in the documents listed in Sections 2.2 and 2.3 above.

1. The PCB vendor's capability should be reviewed and assessed for manufacturability of designs.

5.5.5 When the system developer or supplier will use existing board lots to manufacture printed wiring assemblies or use previously manufactured assemblies, such hardware shall be accepted via review and approval by the Project CSO and the GSFC MPCB CRAE. The review will consist of mission environmental constraints and the board or assembly handling and storage history. The MPCB CRAE will assess the risk (if applicable) associated with the use of the existing board lots or assemblies for the Project office to make final determination.

5.5.6 A design review of the complete circuit board assembly should precede PCB assembly process. Risk mitigations shall be defined and documented for requirements herein that cannot be met due to the lack of availability of procurement specifications, test samples, test data or other required evidence of quality assurance. Risk mitigations shall be approved by the Project CSO or the CSO's representative. The project CSO or their delegate shall record that the PCBs are inherited designs, or build-to-print designs for each affected subsystem in the Supplier Insight module of Meta (https://meta.gsfc.nasa.gov/).

5.5.7 The system developer or supplier shall facilitate a review of non-standard PCB designs, or PCB designs that include non-standard features (see 5.2), that are not covered by the IPC-2220 and IPC-6010 series. The Project CSO or the CSO's representative shall be part of this review. Evaluation should be based on mission risk, heritage of use, and test/qualification data that supports the reliability of the non-standard PCB design for use in applicable hardware.

6. PROCESSING

6.1 Assurance and Reviews

1. This standard shall be imposed, with or without exceptions or additions approved by the Project Chief Safety and Mission Assurance Officer (CSO), for all PCBs that will be employed under this standard for missions required to follow NPR 7120.5.
2. Project mission assurance documentation (e.g., the Mission Assurance Requirements [MAR] section of the contract statement of work for out-of-house production or the mission assurance implementation plan for GSFC in-house production) shall specify the applicable mission risk class when invoking this standard.
3. The CSO or the Code 300 SMA Technical Authority shall approve PCB lots prior to board assembly.
4. The Project CSO or their delegate is responsible for reviewing the structural integrity evaluation results and recommending acceptance or rejection of the lot. Successful completion of the structural integrity analysis, both by the PCB vendor (per 6.5) and by the third-party structural integrity testing lab (per 6.6.2), forms the basis for the system developer or supplier to accept delivery of the PCB lot. The review and recommendation shall be included in the PCB Lot Acceptance and Quality Conformance Testing Results. See 6.4.3 for non-conforming lots.
5. The GSFC Safety and Mission Assurance Directorate (Code 300) shall be the technical authority for PCB quality assurance and shall be responsible for interpreting the intent for each requirement stated herein and for approval of related waivers. Approved waivers shall be included in the lot data acceptance package.

6.2 Printed Circuit Board Procurement

6.2.1 Flow down of Manufacturing and Quality Requirements

PCB procurements shall impose on the PCB vendor all applicable requirements defined herein and in applicable project quality assurance requirements documents that are related

to realization of the PCB design and intended performance, manufacturing materials and processes, requisite tests and inspections, quality assurance, data delivery, data retention, and test coupon delivery. These requirements and specifications may be represented in drawing notes as well as in procurement documentation such as a purchase order or contract and shall include:

1. All additions and exceptions to the baseline design requirements in 5.1.
2. All additions and exceptions to the baseline manufacturing quality requirements in 6.3.3.
3. All additional design and quality assurance requirements defined in Section 6.3.4.
4. All additional design and quality assurance requirements defined by project-specific, approved requirements documents.
5. Use of DC Current Induced Thermal Cycling Test per 6.5.2 when applicable.

6.2.2 Qualified Vendors

A PCB vendor qualification and assessment shall be carried out based on criteria identified in IPC-6011. The extent of the qualification and assessment shall be commensurate with the requirements of the quality criteria identified in the applicable IPC-6010 series standards. For mission risk Class A and Class B, the system developer or supplier shall have performed a source inspection of the vendor's manufacturing capability and reviewed production lot quality history within the prior two years. An additional one-year grace period to receive periodic reviews may be permitted if approved by the project.

6.2.3 PCB Test Coupons

1. Procurement documentation shall specify that sufficient quantities of coupons shall be built into the production panel to satisfy needs for vendor acceptance coupon testing per 6.5.1 as well as third-party coupon testing per 6.6.1. See 6.2.6.
2. Procurement specifications shall direct the PCB vendor to ship the test coupons defined in 6.2.6 to GSFC or to a GSFC-assessed third-party PCB coupon test lab for analysis in accordance with 6.6. The GSFC PCB Coupon Submittal Form (GSFC Form 23-16) shall be used for submitting PWB test coupons that are directly traceable to each board used in flight hardware and are submitted to the GSFC or to a GSFC-approved laboratory for structural integrity evaluation. The GSFC Form 23-16 constitutes a minimum set of information required.
3. Procurement specifications should define optional acceptance tests, when applicable. For a list of optional acceptance tests, see 6.5.2.

4. For mission risk classes A and B per GPR 8705.4, PCB test coupons shall be generated and provided to the GSFC or a GSFC-assessed third-party laboratory for structural integrity evaluation. This requirement is optional for mission risk classes C, D, and Sub-D.

6.2.4 Delivery of PCB Lots

Procurement requirements shall specify to the vendor that procurement documentation, PCB lot data, and structural integrity test coupons be delivered prior to the delivery of the finished boards.

1. The acceptability of the lot is predicated on the compliance and acceptability of the lot data.
2. For mission classes D or Sub-D per GPR 8705.4, the system developer or supplier may “at risk” populate PCB concurrently or after the printed circuit board structural integrity coupons are inspected at GSFC Laboratory or at a third-party laboratory.
3. All PWB test coupons provided to GSFC or to a GSFC-assessed third-party laboratory shall be directly traceable to each board used in flight hardware.
4. Risk assessments, as discussed in 7.6, are performed for coupons that exhibit nonconformance to requirements. If the risk assessment indicates elevated risk due to the nonconformance, then use of the board(s) shall be dispositioned by MRB as a major nonconformance. Vendors shall be responsible for replacing PCB lots that are not accepted by the GSFC project. Boards should not be rebuilt without a determination of the cause for the nonconformance, including whether the cause traces to a problem in the design, specification, or flowdown of requirements.
5. Neither test coupons nor finished boards shall be delivered for lots that fail to pass vendor acceptance testing as defined in 6.5.1.
6. When the system developer or supplier will use existing board lots or previously manufactured assemblies, see section 5.5.5.

6.2.5 Lot Information and Data

Procurement requirements shall specify that the PCB vendor submit the following information and data for each board lot. The following lot information and data shall be included in the lot data acceptance package:

1. The panel map
2. PCB drawings
3. Drill chart
4. PCB stackup
5. Specification of base material construction
6. Location of holes and features when board is submitted in lieu of test coupons (see 6.2.64)
7. IPC-6010 series PCB vendor acceptance test and periodic data. The PCB vendor shall provide the results, in the form of data, for all verification tests required by the applicable IPC-6010 series standard and section 6.3.3 herein. The delivered results shall provide resolution that is commensurate with the requirement (e.g., quantitative if the requirement is quantitative, "pass/fail" if the requirement is defined in this manner).
8. Data shall be supplied for the most recent acceptance and quality conformance testing performed per the frequencies prescribed in the applicable procurement specification.

For example, requirements listed in section 4, table 4-3, and table 4-4 of IPC-6012. The microsections associated with vendor acceptance testing shall be made available to the Project upon request.

a. Results of external visual inspection (6.7)

6.2.6 Test Coupons for Third-Party Structural Integrity Testing

1. The sample size of coupons for third-party analysis is dependent upon the layer count of the represented PCBs.
   a. For single-sided PCBs, coupons are not required.
   b. For double-sided PCBs, a set of coupons shall be provided for evaluation per production lot date code.
   c. For multilayer PCBs (three or more layers), a set of coupons shall be provided for evaluation per production panel.

2. The minimum set of coupons, as defined by IPC-2221, necessary to complete third-party structural integrity testing shall be:
   a. One (1) A and one (1) B, or
   b. Two (2) A/B, or
   c. Two (2) AB/R
   d. If any printed board on the testing panel contains a blind via, buried via, and/or microvia, an additional B or A/B coupon duplicating each contained feature shall be provided.
   e. If ENIG or ENEPIG are used as a final finish, any one of the following coupons shall be provided: C, M (preferred), or P If the PCB vendor provides quantitative results of ENIG or ENEPIG surface finish thickness for the coupons associated with a lot, those results may be used in lieu of M coupon third party testing of surface finish.
   f. Assurance requirements for printed circuit boards that use OSP (organic solderability preservative) shall be identified in the procurement documentation.
   g. For surface finishes other than ENIG and ENEPIG, requirements for inspection and acceptability shall be identified in the procurement documentation.

3. Custom coupons may be submitted instead of those required in 6.2.6.2 above. Custom coupons shall comply with IPC-2221 and contain, at a minimum, two sets of three holes, one in the X and one in the Y dimensional planes, as well as a set of three holes to evaluate blind, buried, and micro via structures if contained in the represented panel. If ENIG or ENEPIG are used as a final finish, the coupon shall contain a pad with minimum size of 0.060 in x 0.060 in for the plating measurement.

4. A qualification board may be submitted instead of the coupons required in 6.2.6.2 above provided the qualification board complies with IPC-2221 and contains, at a minimum, two sets of three holes, one in the X and one in the Y dimensional planes, as well as a set of three holes to evaluate blind, buried, and micro via structures if contained in the represented panel. The location of the holes and features to be evaluated shall be provided by the vendor. If the PCB vendor provides quantitative results of ENIG or ENEPIG surface finish thickness, those results may be used in lieu of qualification board third party testing of surface finish.

6.3 Manufacturing Quality Requirements

6.3.1 Bare PCBs shall not be populated prior to approval by the Project office.

6.3.2 Master Drawings and CAD Files
If there is a discrepancy between the master drawing and the CAD files, the vendor shall obtain verification from the PCB procuring agent regarding the correct design to be fabricated. The procuring agent shall obtain concurrence from the designer when providing clarifications about design files to the PCB vendor.

6.3.3 Quality Standard

PCBs shall be manufactured and tested in accordance with the requirements of IPC-6011, Generic Performance Specification for Printed Boards, and the relevant quality standards shown in a. through d. below. Use of a revision of these standards that is not in the project's MAR or contract, or an alternate standard (e.g., military, European Space Agency) is considered a departure from this standard (see 7).

1. IPC-6012 Space Addendum, Space and Military Avionics Applications Addendum to IPC-6012, Qualification and Performance Specification for Rigid Printed Boards
2. IPC-6013, Qualification and Performance Specification for Flexible Printed Boards
3. IPC-6015, Qualification and Performance Specification for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures
4. IPC-6018 Space Addendum, Space and Military Avionics Applications Addendum to IPC-6018, Qualification and Performance Specification for High Frequency (Microwave) Printed Boards

6.3.4 Additional Manufacturing Requirements

The following requirements shall be applied for designing, fabricating and testing PCBs, in addition to or with precedence over the requirements in the IPC-6010 series specifications and drawings.

1. Board Markings

    a. All traceability markings of PCBs and coupons should be non-conductive white epoxy base ink, low outgassing formulation (1% TML / 0.1% CVCM IAW ASTM E595).
    b. Labels shall not be used to identify flight boards or coupons.
    c. Solder on copper for marking is not preferred.

2. Etchback

    a. Negative etchback shall not be allowed unless evidence is submitted, that is reviewed and approved by the Project CSO in consultation with the MPCB CRAE, demonstrating that residue is sufficiently controlled in the desmearing process and/or interconnect stress testing indicates that the finished boards will not contain

trapped residues that limit service life.

b. When no etchback condition is specified on the drawing, criteria for smear removal shall be applied for product acceptance.

3. Plating Folds

a. Plating folds and inclusions shall be enclosed.

4. Annular Ring - Filleting or "Tear Drops"

a. Employment of filleting or "tear drops" is permissible, but does not relieve vendors of the minimum external annular ring or breakout requirements.

5. Solderability

a. For bare PCBs that have been stored for a period of more than six months after fabrication, a surface and plated-through-hole solderability test shall be performed.

b. Surface and plated-through-hole solderability shall be evaluated in accordance with J-STD-003, Category 2.

6. Wire Bond Pad Surface Finish Roughness

a. The maximum surface roughness in the pristine area of wire bond pads shall be measured in accordance with IPC-TM-650, Method 2.4.15 with a roughness-width cutoff of 80% of the maximum length of the wire bond pad.

7. Electrical Test Requirements

a. Requirements for impedance and isolation testing should be indicated in the drawing notes, when applicable.

8. Microsection Process

a. When thermal stress preconditioning is required, test coupons shall be thermally stressed per IPC TM-650 method 2.6.8 Test Condition A prior to microsectioning.

b. For certain PCB designs, for example, double-sided flex cables, the thermal ranges defined in IPC TM-650 method 2.6.8 Test Condition A may be excessive. Deviations from requirement in 6.3.4 (h) (i) shall be approved by the GSFC Project.

c. Microsection procedure, examination, and evaluation shall be performed per IPC TM-650 method 2.1.1.

6.4 GSFC Product Acceptance Requirements

1. All data that are reviewed to determine lot acceptability are collected in the lot data acceptance package. See Appendix A for Data Item Deliverables (DIDs) pertaining to mission classes A through D. The vendor acceptance test data will be reviewed to ensure

compliance with the requirements imposed by the procurement documents including those imposed by the PCB drawing notes.

6.4.2 GSFC shall perform lot acceptance by:

1. Reviewing the delivered vendor acceptance test data package. See sections 6.2.5 and 6.2.6 for lot data acceptance details for PCB procurement.
2. Performing an external visual inspection of each delivered PCB.
3. Reviewing the DC Current Induced Thermal Cycling Test results, in accordance with 6.5.2, when specified by the Project, to augment PCB vendor or third-party structural analysis results.
4. A final signoff by the Project CSO.

6.4.3 Handling of Non-conformances

When delivered data, either from testing or structural integrity analysis, reveals a nonconformance, a risk assessment is performed as discussed in 7.6. Use of a non-conforming lot shall be recorded by the Project or GSFC SMA and noted in the GSFC Meta system, and any risk included to the record. Final dispositions for PCBs that do not conform to applicable requirements will come from the GSFC Project Office.

6.5 Vendor Product Acceptance Testing

Quality assurance for PCBs used in applicable hardware consists of ensuring conformance with baseline manufacturing quality standards, additional quality and performance criteria defined herein, in the PCB drawing notes, and in project-specific requirement documents. Quality conformance is evaluated through inspections and tests performed on the boards that will be used in the mission as well as on representative samples of those boards, called coupons.

6.5.1 IPC-6010 Vendor Acceptance Testing

1. The PCB vendor should perform acceptance testing to verify quality conformance of each production panel and represented board. For rigid printed boards, vendor acceptance testing shall be per IPC-6012 Space Addendum. For flexible printed boards, vendor acceptance testing shall be per IPC-6013, Table 4-3. For MCM-L boards, vendor acceptance testing shall be per IPC-6015, Table 4-1. For high frequency boards, vendor acceptance testing shall be per IPC-6018, Table 4-3.
2. The vendor shall conduct thermal shock tests and destructive physical analysis (DPA) as specified in the Special Requirements section of the applicable IPC-6010 series specification.

6.5.2 Optional Acceptance Testing

The Project may require a DC Current Induced Thermal Cycling Test as a requirement or as an option for evaluating design reliability and lot quality when boards will not comply with the requirements herein by design.

1. The Project may require DC Current Induced Thermal Cycling Test results in order to

perform a risk assessment in cases where test result non-conformances are observed.

2. When DC Current Induced Thermal Cycling Testing is required, the system developer or supplier shall ensure that testing is in accordance with IPC-TM-650, Method 2.6.26 and the test results are delivered to GSFC for review and are included in the lot acceptance data package.

6.6 Third-Party Test Coupon Structural Integrity Analysis

6.6.1 General

1. All submitted lots shall be evaluated for structural integrity by coupon microsection analysis with the exception of lots of single and double-sided boards. This evaluation is in addition to the coupon microsection analysis required by 6.5.1.
2. Third-party structural integrity analysis shall be performed by the GSFC Materials Engineering Branch (MEB) coupon laboratory or by a third-party structural integrity analysis testing lab that has been evaluated by GSFC to perform this testing.
   a. Use of a third-party structural integrity analysis testing lab that has been evaluated by GSFC for structural analysis shall be at the discretion of the Project.
   b. Prime or subcontractors who seek to comply with the requirements herein by using a third-party structural integrity analysis testing lab shall obtain approval to do so in advance, from the Project.
   c. Testing facilities shall not perform coupon evaluation in the capacity of a third-party evaluator for coupons that are manufactured at the same or associated facilities.
3. The system developer or supplier shall ensure that the coupons, of the correct type and quantities, the drawing notes for the lot, and lot traceability data including those specified in 6.2.5 as a minimum, are supplied to the assigned analysis lab.
4. The GSFC-assessed third-party structural integrity analysis lab shall only receive work instructions or directions from GSFC.

6.6.2 Structural Integrity Analysis

1. The third-party structural integrity analysis lab shall review the delivered lot information (see 6.2.5.1, 6.2.5.8, 6.2.6) prior to the start of the structural integrity evaluation.
2. The third party structural integrity analysis lab shall examine microsections in the as-received condition in the X dimensional plane and in the thermally stressed condition in the Y dimensional plane. Test coupons containing blind, buried, or microvias shall also be evaluated in the thermally stressed condition.
3. Test coupons shall be inspected for structural integrity in accordance with the criteria in the procurement requirements (see 6.2.1). This requirement assumes that the procurement requirements reflect a reviewed and approved design, reviewed and approved drawing notes, and do not conflict with the quality criteria herein without prior approval by the CSO.
4. Microsections shall be prepared per IPC-TM-650, Method 2.1.1, or a process that is documented and evaluated during the third-party structural integrity analysis testing lab assessment process.
   a. Material with a room temperature-cure shall be used to pot samples; hot mount epoxy shall be prohibited.

b. Traceability to the PCB serial number shall be maintained on the coupon or sample throughout the microsection preparation and inspection processes.
c. The following quality characteristics of the finished microsection shall apply:
d. The potting material shall completely fill PTHs.
e. There shall be no gaps between the potting material and the sample.
f. Microsections shall be free of excessive scratches and smear.

5. Microsections shall be examined and evaluated per IPC-TM-650, Method 2.1.1.

6.6.3 Structural Integrity Evaluation Reporting and Retention

1. The results of the structural integrity examination and evaluation shall be included in the PCB Lot Acceptance and Quality Conformance Testing Results (per DID B).
2. The third-party structural analysis report shall not characterize the overall results of the structural analysis as a pass or fail. This is to prevent the mischaracterization of a non-conformance to qualitative requirements as a functional failure of a populated assembly.

3. The microsectioned coupons and remnants for lots that will be used under this standard shall be retained for a time period defined by the GSFC Mission record retention requirements.
4. The microsectioned coupons and remnants shall be archived by Code 300 (SMA) until mission disposal. All microsectioned coupons and remnants used in assurance shall be provided to Code 300 (SMA).

6.6.4 Structural Integrity Testing Lab Process Data

1. The GSFC coupon lab and all third-party structural integrity analysis labs shall establish and maintain summary data for the structural integrity analyses performed to the requirements herein for GSFC Projects. This summary data shall be made available to GSFC Microelectronics Packaging and Circuit Board CRAE upon request. The data shall include the following at a minimum for each coupon submission:
i. Unique identifier representing the coupon submission, received date, and structural integrity analysis report
ii. GSFC Project and subsystem associated with the coupon submission
iii. PCB Vendor (Name and CAGE code or address)
iv. Lot identifier
v. Applicable specification or standard (IPC or other fabrication standard if applicable)
vi. Applicable performance classification
vii. Board information
(1) Number of layers
(2) IPC-6010 series defined board type (if IPC standards are applicable)
(3) Base material
(4) Surface plating material
(5) Board interconnect types used (blind via, buried via, via-in-pad, wirebonding, etc.)
viii. Defects or non-conformances found (if any)

2. The GSFC coupon lab and all third-party structural integrity analysis labs should employ through-put metrics that are reported to GSFC Microelectronics Packaging and Circuit

Board CRAE on a quarterly basis. The testing lab should assess:

i. Time that coupon submissions are in the queue prior to start of the evaluation

ii. Time from start of evaluation to report completion

iii. Time from report completion to report delivery

6.7 Incoming External Visual Inspection

1. PCBs delivered shall be optically inspected at the assembly facility to verify that they comply with the procurement specification (see 6.2.1, 6.3.4). The inspection shall be performed by a certified PCB inspector, in accordance with 4.3, and the results shall be submitted to the Project CSO for inclusion in the PCB Lot Acceptance and Quality Conformance Testing Results.

2. PCBs that fail to meet the external visual inspection quality criteria defined in the procurement requirements shall be segregated from conforming product at inspection and identified as non-conforming. A risk assessment may be performed for PCBs that fail to meet external visual inspection quality criteria defined in the procurement documents. Final directions for PCBs that fail to meet external visual inspection quality criteria will come from the Project CSO.

6.7.2 PCB Handling, Storage and Retention Requirements

a. IPC-1601 or a supplier established and GSFC approved handling and storage procedure shall be used by all participants in the PCB supply chain for identifying procedures and practices of PCB handling and storage.

b. PCBs that are not handled and stored per the appropriate requirement shall be segregated from conforming product and identified as non-conforming. A risk assessment may be performed for PCBs that fail to meet the handling and storage requirement. Final directions for the use of PCBs that fail to meet PCB handling and storage requirements will come from the Project CSO.

c. Production PCBs shall be retained by the supplier for a time period defined by the Project.

d. For bare PCBs which are intended to be used after having been stored for a period of more than six months after fabrication, the solderability testing per 6.3.4.5 shall be conducted at the time of use.

7. DEPARTURES FROM THIS STANDARD

7.1 Departures

All departures from this standard shall be approved via the Project waiver process. The Project CSO shall consult the GSFC Microelectronics Packaging and Printed Circuit Board (MPCB) Commodity Risk Assessment Engineer (CRAE) in all waiver processes.

7.2 Post-Production Testing

Post-production testing alone, whether on finished boards or representative test coupons, shall not be recognized as a substitute for meeting the design, procurement, manufacturing, and quality assurance requirements herein.

7.3 Non-conforming Product

Documentation of proposed repair or other methods used for risk mitigation for procurement of lots

known to not be in conformance with the requirements herein shall be provided to the Project CSO and the GSFC MPCB CRAE for approval.

7.4 Non-conforming Product Disposition

Any non-conformance for which a risk assessment indicates an elevated risk shall be dispositioned either through MRB or another project process to adopt the risk and decide on mitigations. The Project CSO is responsible for convening an MRB that includes the SMA and engineering PCB technical experts and the Project's reliability engineer. Use of a non-conforming lot that has elevated risk shall have the associated risk brought to the project risk board and recorded in the GSFC Meta system.

7.5 Third Party Lab Submission

All coupon reports generated at a GSFC assessed third party laboratory shall be submitted to the GSFC MPCB CRAE. The submittal to the GSFC MPCB CRAE fulfills two purposes: It allows for an independent assessment of the coupon report before the report is released to the Project, and it facilitates the performance of a risk assessment.

7.6 Risk Assessments

A risk assessment shall be performed prior to further action for reports that indicate nonconformance to requirements. Final dispositions for PCBs with non-conforming structural integrity coupons will come from the GSFC project. See section 4 for information on delivery of PCB coupons.

APPENDIX A: EXAMPLE DATA ITEM DELIVERABLES (DID)

The following DIDs are recommended for use in Project MARs in accordance with the requirements of this standard.

Note that the following DIDs apply to a Class A or B mission.

DID A Alternate Printed Circuit Board (PCB) Standard Declaration

Title: Alternate Printed Circuit Board (PCB) Standard Declaration	DID No.: A
MAR Paragraph: x.x.x	
Use: Alternate printed circuit board standards for design, manufacturing instructions, or quality test and inspection criteria are reviewed for risk exposure to the project and suitability for flight, flight spare and custom mission critical support hardware.	
Reference Documents: - GSFC-STD-8001 Standard Quality Assurance Requirements for Printed Circuit Boards - IPC-2221 Generic Standard on Printed Board Design (Class 3) - IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards (Class 3) - IPC-2223 Sectional Design Standard for Flexible Printed Boards (Class 3) - IPC-2225 Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies (Class 3) - IPC-6011 Generic Performance Specifications for Printed Boards (Class 3) - IPC-6012 Qualification and Performance Specification for Rigid Printed Boards (Class 3/A) - IPC-6013 Qualification and Performance Specification for Flexible Printed Boards (Class 3) IPC-6015 Qualification and Performance Specification for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures (Class 3) - IPC-6018 Microwave End Product Board Inspection and Test (Class 3 or 3/A) - MIL-PRF-55110 Performance Specification Printed Wiring Board, Rigid, General Specification For - MIL-PRF-31032 Performance Specification Printed Circuit Board/Printed Wiring Board, General Specification For	
Place/Time/Purpose of Delivery: - When an alternate standard or criteria as defined by 6.3.3 of GSFC-STD-8001 has been used or will be used to design, manufacture, test, or inspect PCBs for flight, flight spare and custom mission critical support hardware, the supplier shall provide the Program office a report of that alternate standard or criteria for GSFC review and approval. - The report shall include the full requirements set and indicate any items that are not explicitly specified within the alternate standard (i.e., designer's decisions) or are exceptions to the standard default requirements.	
Preparation Information:	

Notify GSFC or the GSFC-certified testing lab regarding shipment of alternate standard report.

DID B PCB Lot Acceptance and Quality Conformance Testing Results

Title: PCB Lot Acceptance and Quality Conformance Testing Results	DID No.: B
MAR Paragraph: x.x.x	
Use: Data results of printed circuit board lot acceptance and quality conformance testing are evaluated to verify supplier compliance to quality assurance requirements.	
Reference Documents: - GSFC-STD-8001 Standard Quality Assurance Requirements for Printed Circuit Boards - IPC-6011 Generic Performance Specifications for Printed Boards - IPC-6012 Qualification and Performance Specification for Rigid Printed Boards - IPC-6013 Qualification and Performance Specification for Flexible Printed Boards IPC-6015 Qualification and Performance Specification for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures - IPC-6018 Microwave End Product Board Inspection and Test - MIL-PRF-55110 Performance Specification Printed Wiring Board, Rigid, General Specification For - MIL-PRF-31032 Performance Specification Printed Circuit Board/Printed Wiring Board, General Specification For	
Place/Time/Purpose of Delivery: - Testing results shall be delivered as soon as practicable following board fabrication and prior to PWA population. - The microsections associated with supplier acceptance testing shall be made available to the Project upon request.	
Preparation Information: The supplier shall deliver to the Program office the lot data acceptance package, for all verification tests required by and defined in the standard and the procurement instructions imposed on the PCB vendor by the supplier. The delivered results shall provide resolution that is commensurate with the requirement (e.g., quantitative if the requirement is quantitative, "pass/fail" if the requirement is defined in this manner). Notify GSFC regarding shipment of testing data package. The lot data acceptance package shall be assembled as a record of the PCB lot's compliance with the requirements of GSFC-STD-8001 and as a minimum include:	

i. Additions or exceptions to the requirements herein
ii. Approved waivers
iii. Design review results
iv. Drawing and Drawing Notes
v. Lot information and supplier acceptance test data
vi. Review of supplier acceptance test data by GSFC
vii. Test coupon information
viii. Structural integrity analysis report
    a. Unique report identifier
    b. Date of report
    c. Revision number of report
    d. Accept/reject criteria used
    e. Test data, citing the number, type and location of defects and non-conformances observed
    f. Photographs with scale of cited non-conformances observed
    g. Traceability of defects and non-conformances found to the parent panel
    h. Anomalies discovered which are not defined in the procurement requirements
    i. Pictures with measurement of any cited non-conformances
    j. Final result of the analysis: Conforming or Non-conforming
ix. Results of incoming visual inspection of PCBs
x. Approval by GSFC SMA for acceptance of the PCB lot when applicable

DID C Printed Circuit Board (PCB) Test Coupons

Title: Printed Circuit Board (PCB) Test Coupons	DID No.: C
MAR Paragraph: x.x.x	

Use:

PCB test coupons are evaluated to validate that the represented PCBs meet the structural integrity requirements deemed suitable for use in space flight and mission critical ground applications.

Reference Documents:

- GSFC-STD-8001 Standard Quality Assurance Requirements for Printed Circuit Boards
- IPC-2221 Generic Standard on Printed Board Design
- IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards
- IPC-2223 Sectional Design Standard for Flexible Printed Boards
- IPC-2225 Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies
- IPC-6011 Generic Performance Specifications for Printed Boards
- IPC-6012 Qualification and Performance Specification for Rigid Printed Boards
- IPC-6013 Qualification and Performance Specification for Flexible Printed Boards
- IPC-6015 Qualification and Performance Specification for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures
- IPC-6018 Microwave End Product Board Inspection and Test
- MIL-PRF-55110 Performance Specification Printed Wiring Board, Rigid, General Specification For
- MIL-PRF-31032 Performance Specification Printed Circuit Board/Printed Wiring Board, General Specification For

Place/Time/Purpose of Delivery:

- Coupon specimens do not need to be submitted for single-sided printed wiring boards, shall be submitted per lot for double-sided boards, and shall be submitted per panel for all other board types.
- The system developer or supplier shall provide one A and one B, or two A/B coupons, or one AB/R coupon per IPC-2221 for both unstressed and thermally stressed coupon evaluation for structural integrity by GSFC or a GSFC-assessed testing lab. If the represented PCB design contains a blind, a buried, and/or a micro via, the system developer or supplier shall provide an additional B or A/B coupon duplicating each contained feature for thermally stressed evaluation.
- If ENIG or ENEPIG are used as a final finish, any one of the following coupons shall be provided: C, M (preferred), or P If the PCB vendor provides quantitative results of ENIG or ENEPIG surface finish thickness for the coupons associated with a lot, those results may be used in lieu of M coupon third party testing of surface finish.
- The system developer or supplier may submit either custom coupons or qualification boards in lieu of the aforementioned coupons. Custom coupons shall comply with IPC-2221 and contain, at a minimum, two sets of three holes, one in the X and one in the Y dimensional

planes, as well as a set of three holes to evaluate blind, buried, and micro via structures if contained in the represented panel. If ENIG or ENEPIG are used as a final finish, the coupon shall contain a pad with minimum size of 0.060 in x 0.060 in for the plating measurement.

- The system developer or supplier shall provide supporting manufacturing documentation with the coupons that is traceable to the flight boards, including the performance specification and product classification to which the board was fabricated; type of printed board; board drawing or drawing notes; relevant deviations, waivers, or additional fabrication requirements; panel map; indication if there are blind, buried, or micro vias present; number of board layers; base material information; PCB part number and revision level; lot date code; serial number and Vendor ID (CAGE Code if a US vendor).
- In the case that a GSFC-assessed testing lab is used, the system developer or supplier shall deliver the test results to GSFC with the end item data package. The system developer or supplier shall deliver all the coupon remnants and microsections to GSFC.
- Use of a GSFC-assessed testing lab must be approved by the Project CSO.

Preparation Information:

Notify GSFC or the GSFC-assessed testing lab regarding shipment of PCB test coupons.

DID D Printed Circuit Board (PCB) Coupon Evaluation Report

Title: Printed Circuit Board (PCB) Coupon Evaluation Report	DID No.: D
MAR Paragraph: x.x.x	
Use: PCB test coupons are evaluated to validate that PCBs are suitable for use in space flight and mission critical ground applications. The laboratory report provides the information needed to decide to use the PCBs associated with the coupons. The laboratory report also necessitates a risk assessment when non-conformances are observed.	
Reference Documents: - GSFC-STD-8001 Standard Quality Assurance Requirements for Printed Circuit Boards - IPC-6011 Generic Performance Specifications for Printed Boards - IPC-6012 Qualification and Performance Specification for Rigid Printed Boards - IPC-6013 Qualification and Performance Specification for Flexible Printed Boards - IPC-6015 Qualification and Performance Specification for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures - IPC-6018 Microwave End Product Board Inspection and Test - MIL-PRF-55110 Performance Specification Printed Wiring Board, Rigid, General Specification For - MIL-PRF-31032 Performance Specification Printed Circuit Board/Printed Wiring Board, General Specification For	
Place/Time/Purpose of Delivery: - The system developer or supplier shall deliver test coupon reports for conforming or non-conforming product to GSFC as soon as practicable for information and review. - In the case that a GSFC-assessed testing lab is used, the system developer or supplier shall deliver the test results to GSFC with the end item data package. The system developer or supplier shall deliver all the coupon remnants and microsections to GSFC.	

Preparation Information:

The supplier shall provide reports from GSFC or a GSFC-assessed laboratory for PCB test coupons that are directly traceable to each board that is intended for use in hardware for evaluation:

- The supplier should use the GSFC Coupon Submittal Form (GSFC 23-16) for documentation and delivery of design characteristics associated with the coupon report.
- If the GSFC Coupon Submittal Form (GSFC 23-16) is not used, the system developer or supplier shall provide supporting manufacturing documentation with the coupons that is traceable to the flight boards, including the performance specification and product classification to which the board was fabricated; type of printed board; relevant deviations, waivers, or additional fabrication requirements; indication if there are blind, buried, or micro vias present; base material information; PCB part number and revision level; lot date code; serial number and Vendor ID (CAGE Code if a US vendor).
- The submittal package shall include a copy of the board drawing or drawing notes; stackup, panel map; and number of board layers if not otherwise included.

Note: Final dispositions for populating PCBs after structural integrity coupon analysis will come from GSFC project.

DID E Printed Circuit Board Procurement Plan

Title: Printed Board Procurement Plan	DID No.: E
MAR Paragraph: x.x.x	

Use:

Supplies information that will be used to verify requirements, indicate manufacturing readiness, and determine additional assurance methods as necessary.

Reference Documents:

- GSFC-STD-8001 Standard Quality Assurance Requirements for Printed Circuit Boards
- IPC-2221 Generic Standard on Printed Board Design
- IPC-6011 Generic Performance Specifications for Printed Boards
- IPC-6012 Qualification and Performance Specification for Rigid Printed Boards
- IPC-6013 Qualification and Performance Specification for Flexible Printed Boards
- IPC-6015 Qualification and Performance Specification for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures
- IPC-6018 Microwave End Product Board Inspection and Test
- MIL-PRF-55110 Performance Specification Printed Wiring Board, Rigid, General Specification For
- MIL-PRF-31032 Performance Specification Printed Circuit Board/Printed Wiring Board, General Specification For

Place/Time/Purpose of Delivery:

- Provide preliminary information on flight printed boards thirty (30) days prior to CDR for approval.
- Provide changes to the plan a minimum of fourteen (14) days prior to printed board manufacturing for approval.

Preparation Information:

For all printed boards to be used in flight, flight spare and custom mission critical support hardware, the procurement plan shall contain:

- Name of next higher level assembly (box or subsystem)
- Printed board assembly name
- Part number and revision level
- Indication as being a new or heritage design
- Description of design complexity, to include:
  - Number of layers
  - Overall board thickness
  - Most complex via stack-up
  - Use of micro-vias
  - Use of via-in-pad
  - Line width and spacing
  - Maximum voltage in application
  - Base material (IPC-4101 designation or trade name)
  - Applicable printed board design standard

    - Applicable printed board performance standard
    - Fabrication notes or procurement specifications
- Note of any waiver or deviation affecting printed board requirements or acceptability
- Printed board vendor(s) or candidates
- Quantity required for flight build
- Minimum quantity required for spares

The procurement information will ensure that boards and test coupons are fabricated for each design in a quantity sufficient to meet testing requirements per IPC-2221 Generic Standard on Printed Board Design and satisfy vendor acceptance testing per IPC-601X.