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Area Array Package Assembly and Manufacturing Practices for Flight Hardware

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FOREWORD

This standard is published by the Goddard Space Flight Center (GSFC) to provide uniform engineering and technical requirements for processes, procedures, practices, and methods that have been endorsed as standard for NASA programs and projects, including requirements for selection, application, and design criteria of an item.

This standard establishes requirements which apply to all uses on flight hardware of area array packaged electronic parts which are solder-attached to printed circuit boards with high temperature solder columns, balls, springs, or other area array attachment technologies. The requirements address as-received part inspection, printed circuit board design, manufacturing process and quality control, process inspection points, inspection techniques and associated inspection criteria, rework, and process control validation testing. These requirements do not address subassembly-level design qualification.

Requests for information, corrections, or additions to this standard should be submitted via "Feedback" in the GSFC Technical Standards System at https://standards.gsfc.nasa.gov.

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1. SCOPE

1.1 Purpose

The purpose of this standard is to provide requirements and recommendations intended to facilitate production of defect-free area array solder joint interconnects to printed circuit boards intended for use in Flight, Flight Spare and Custom Mission Critical Support Hardware applications. This standard does not provide application specific reliability test requirements (e.g. qualification requirements).

1.2 Applicability

This standard is applicable to all uses on Flight, Flight Spare and Custom Mission Critical Support Hardware of area array packaged electronic parts that are solder-attached to printed circuit boards with solder columns, balls, springs, or other area array attachment technologies.

1.3 Risk Classes per GPR 8705.4

Requirements herein that are unique to a certain mission risk class (e.g., Class C or Class D) shall be applied in accordance with the mission risk classification as assigned by NASA Headquarters or other stakeholder as applicable. Requirements herein that are not associated with a particular mission risk class are applicable to all mission risk classes.

1.4 In-house vs. Out-of-house

This standard applies in total for in-house projects at GSFC and out-of-house projects to the extent that it is called out from a directive or project document, such as the project MAR.

1.5 Order of Precedence

This standard establishes quality requirements for the attachment of area array packages to PCBs but does not supersede nor waive established Agency requirements found in other documentation. Where there are conflicts between the requirements found in this standard and the standards in Section 2, the requirements of this standard take precedence.

2. APPLICABLE DOCUMENTS

2.1 General

The documents listed in this section contain provisions that constitute requirements of this standard as cited in the text of Section 4, Requirements. The latest issuances of cited documents shall be used unless otherwise approved by the assigned Technical Authority. The applicable documents are accessible via the NASA Technical Standards System (NTSS) at http://standards.nasa.gov, directly from the Standards Developing Organizations, or from other document distributors.

2.2 Government Documents

GPR 8705.4	Risk Classification Guidelines and Risk-Based SMA Practices for GSFC Payloads and Systems
GSFC-STD-7000	General Environmental Verification Standard (GEVS) for GSFC Flight Programs and Projects

MIL-PRF-55110	Performance Specification: Printed Wiring Board, Rigid General Specification For
MIL-PRF-50884	Performance Specification: Printed Wiring Board, Flexible or Rigid-Flex, General Specification For
MIL-STD-883	Test Method for Microcircuits, Method 2009
NASA-STD-8739.1	Workmanship Standard for Polymeric Application on Electronic Assemblies
NASA-STD-8739.6	Implementation Requirements for NASA Workmanship Standards

2.3 Non-Government Documents

AS9100	Quality Management Systems – Aerospace - Requirements
IPC J-STD-001	Requirements for Soldered Electrical and Electronic Assemblies
IPC J-STD-001S	Space Applications Electronic Hardware Addendum to J- STD-001 Requirements for Soldered Electrical and Electronic Assemblies*
IPC/JEDEC J-STD-033	Handling, Packing, Shipping, and Use of Moisture/Reflow Sensitive Surface Mount Devices
IPC-A-600	Acceptability of Printed Boards
IPC-1601	Handling, Packaging, and Storage of Printed Boards
IPC-6012	Qualification and Performance Specification for Rigid Printed Boards
IPC-6012S	Space and Military Avionics Applications Addendum to IPC-6012x Qualification and Performance Specification for Rigid Printed Boards
IPC-7095	Design and Assembly Process Implementation for BGAs
IPC-7530	Guidelines for Temperature Profiling for Mass Soldering Processes (Reflow and Wave)
IPC-9701	Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments
IPC-TM-650	Test Method for Bow and Twist (Percentage)

2.4 Order of Precedence

The technical requirements of this standard take precedence, in the case of conflict, over the technical requirements cited in applicable documents or referenced guidance documents in Appendix A. In the event of a conflict between the requirements herein and the requirements of the applicable documents or referenced guidance documents, the requirements herein take precedence.

Note: Requirements specified in the drawing or contract take precedence over this standard.

3. ACRONYMS AND DEFINITIONS

3.1 Acronyms

BGA	Ball Grid Array – Surface mount packaging that utilizes a grid pattern of solder balls as interconnects to the printed wiring board.
CGA	Column Grid Array – Surface mount packaging that utilizes a grid pattern of solder columns as interconnects to the printed wiring board.

CCGA	Ceramic Column Grid Arrays – CGAs specifically using ceramic body packaging.
CM	Configuration Management
CTE	Coefficient of Thermal Expansion – Changes in volume of a material as a function of changes in temperature.
DPA	Destructive Physical Analysis
ENIG	Electroless Nickel Immersion Gold
ESD	Electrostatic Discharge
FPGA	Field Programmable Gate Array – A programmable part which is used for data processing.
I/O	Input/Output
LGA	Land Grid Array
MAR	Mission Assurance Requirements – A project-specific mission assurance requirements document that has been formally approved by GSFC Code 300 or the lead Center for Safety and Mission Assurance for the project.
MRB	Material Review Board
MRR	Manufacturing Readiness Review
NSMD	Non-Solder Mask Defined
PDL	Product Design Lead
PR/PFR	Problem Report/Problem Failure Report
PWA	Printed Wiring Assembly – A printed wiring board populated with parts.
PWB	Printed Wiring Board – A substrate that forms the basis for interconnecting components and parts used in a printed wiring assembly, also referred as printed circuit board (PCB)
QTP	Qualification Test Plan
SMT	Surface Mount Technology – A method of mounting electronic parts directly to the surface of a printed wiring board, instead of using through-hole technology. This method is commonly used in today's printed wiring assemblies.

3.2 Definitions

Heritage Hardware Hardware whose design has been previously qualified and used in space applications, and was accepted for use by a NASA program or project.

Inherited Hardware A piece of hardware or hardware design, brought in to a project, that has some amount of prior history, may be built to different design standards, and may not have had NASA insight into the design or construction.

Part Mirroring A practice in PCB design where an area array component is attached directly opposite to an area array component on the other side of the PCB.

PCB Lot One or more boards that are traceable to quality testing and inspection performed on representative samples and coupons.

Supplier An organization or company that provides a product or service to the user under a contract.

System Developer An organization or company that provides a subsystem or subsystem related services to the supplier under contract.

User An organization or company that receives products or services from a supplier under a contract.

4. REQUIREMENTS

4.1 Manufacturing and Quality Control Processes

Manufacturing and quality control processes shall be established and made available for review by NASA. It is recommended that the manufacturing and quality control process address the following:

a. Solder reflow equipment temperature, calibration and reflow profile
b. Parts, materials and board storage and handling
c. Contamination control
d. Solder paste deposition methods and quality control
e. Part placement quality control
f. Proper selection and use of inspection equipment
g. Proper selection and use of assembly cleaning equipment
h. Cleanliness validation controls
i. Failure root cause investigation and corrective action
j. Configuration management (CM) control

4.2 Incoming Parts Inspections

4.2.1 Parts Approval

All area array packaged parts shall meet GSFC project-specific mission assurance requirements (MAR) for part selection and approval prior to use.

4.2.2 Package and Interconnect Documentation

The following information shall be identified and documented on the assembly drawing, parts list, and parts datasheet:

a. Package dimensions
b. Package style
c. Interconnect material(s)
d. Interconnect size and pitch
e. Number of interconnects

4.2.3 Visual Inspection

All area array packages and interconnects shall be inspected prior to installation in accordance with MIL-STD-883, Method 2009.

4.2.4 Bare Board Inspection

In addition to bare board inspection in accordance with IPC-A-600 or equivalent specification identified in the MAR, the following supplemental inspections are specified. The external inspection magnification levels identified in IPC-A-600 should be used. Equipment capable of rendering sufficient resolution and color accuracy should be used.

4.2.4.1 Solder Mask Inspection

Boards should be 100% visually inspected prior to use for any solder mask damage within the area array package land pattern.

4.2.4.2 Board Flatness

Board bow and twist shall be controlled in accordance with the latest revision of IPC-6012 Space Addendum or equivalent.

4.2.4.3 Area Array Package Land Inspection

Boards should be 100% visually inspected in the area array land pattern to identify damage.

4.2.4.4 Area Array Land Pattern Flatness

Each board shall be measured for flatness within the area array land pattern to be within ±0.0015 in across the longest dimension of the area array land pattern. The flatness of the area array land pattern should be evaluated prior to solder paste deposition.

4.2.5 Use of Parts Rejected during Screening

Use of a part (PCB or area array component) that is found to be defective per the screening criteria in Sections 4.2.3, Visual Inspection, through 4.2.4.4, Area Array Land Pattern Flatness, requires review and approval by the Material Review Board (MRB). A risk assessment should be included as part of the MRB.

4.3 Handling, Shipping and Storage of Area Array Packages

The handling, shipping and storage of area array packages shall be per IPC/J-STD-033.

4.4 Printed Circuit Board Design and PWA Design Considerations

4.4.1 Mechanical Design Analysis and Design Approval

Analysis shall be performed to evaluate the integrity of solder joints and interconnects when subjected to on-ground and on-orbit structural and thermal loading. The types of analysis that need to be performed are driven by the on-orbit environment, mission life, design complexity, and heritage use (if any).

The thermo-mechanical analysis should take into account thermal stress that occurs during assembly, on-ground electrical testing, on-ground environmental testing (thermal oven and thermal vacuum testing at the subsystem and spacecraft levels), and various on-orbit scenarios (powered on, powered off, anomalous orientation) as applicable to the mission. The analysis method used should be empirically based and relevant to the designer's area array package size, device pitch, solder material, solder attachment, and board design. The analysis should begin prior to and in parallel with the board design and part placement. The analysis shall be completed prior to and included in the MRR.

For structural and thermo-mechanical analyses, thermal and mechanical designs with features that attach to the top of the part or to the PCB should be included in the assessment. Epoxy added to the package should be included in the analysis. Solder joint fatigue life may be affected by these features.

4.4.2 Inherited and Built-to-Print Design Approval

For products that have either been previously developed and exist (e.g., spares), or will be built-to-print (BTP) or are commercial-off-the-shelf (COTS), the system developer may follow an inherited items review process, in which GSFC shall perform an inheritance risk assessment on the selected

system developer's heritage products, as an alternative to pursuing waivers to a mechanical design analysis.
For inherited products that do not fit the criteria for an inheritance risk assessment, and if any of the following criteria are met, only a structural analysis is recommended to be performed.

a. Design has heritage in terms of the size and pitch of the grid array device.
b. The board design is similar in features, size, and complexity to a board that has flight heritage or has been qualified for space.
c. The structural and thermal environment of the design are enveloped or equivalent to previous missions utilizing a similar board assembly.

The structural analysis should address solder joint fatigue due to board bending (oil canning motion) and loading that would apply shear and bending on the area array interconnection.

4.4.3 Part mirroring

Part mirroring shall require review in preparation to a preliminary design review MRB and approval by the GSFC project.

4.4.4 Solder Surface Finish

Solder lands shall have a tin-lead solder (HASL) or electroless nickel immersion gold (ENIG) finish per IPC-4552. Other surface finishes shall be submitted to the GSFC Project for approval. Requests for the use of solder surface finishes other than HASL or ENIG should be accompanied by a qualification test plan, generated from applicable test and qualification specifications.

4.4.5 Land Geometry

The land diameter shall comply with the part supplier's recommendations or a minimum of 120% of the interconnect diameter in the absence of the part supplier's specification. The land diameter minimum size requirement provides for placement margin and sufficient area for solder deposition. All land design configurations shall be submitted to the GSFC Project for approval. Submissions should include supporting data that is based on risk considerations and trades (including consideration of other options such as use of microvias or relaxing some of the requirements in IPC-6012), heritage of use, and qualification data that supports the reliability of the alternate land designs for use in mission hardware.

4.4.6 Solder Mask

External traces connected to area array interconnect lands shall be covered by solder mask. Area array lands shall be non-solder mask defined (NSMD). The solder mask edge shall not lie inside of the solder land to prevent the edge of the solder mask from creating a stress point in the solder joint.

4.4.7 Shared Via Guidance

Dedicated device pins for power and ground shall use their own individual via (i.e. no sharing of power or ground vias for power distribution). Signal pins that have a common board net (e.g. redundant input, wired-OR output, no connect "NC" tie-offs) may share a neighboring via through a surface trace.

4.4.8 Area Array Package Placement Clearance (Keepout Zone)

Parts surrounding each area array package shall be spaced to allow for sufficient clearance for subsequent rework (e.g., for placement of stencils), visual inspection, application of mechanical staking, placement and rework of decoupling capacitors, and accommodating prototype sockets.

4.4.9 Part Retention

Retention of area array packages such as underfill, corner staking, or corner brackets shall be based on successful qualification testing and shall be detailed on the assembly drawing. Effects of corner staking must be analyzed per Section 4.4.1.

4.4.10 Land Pattern Design Review

Land designs containing fine-pitch (≤1mm) patterns, non-standard patterns, or land patterns where manufacturer-recommended features could not be accommodated shall require a peer design review by the GSFC Project. Compliance with the requirement in this section shall be verified in the design review process. The PWB fabricator should participate in the design for manufacturability peer review.

4.5 **Assembly Qualification Testing**

Assembly qualification tests are tests conducted prior to production of a flight assembly to baseline the design, materials, and processes. Such tests may be used to determine (wear-out period) assembly performance degradation.

A board level qualification basis shall be established by the supplier and reviewed and approved by the GSFC project.

a. For mission classes D or below per GPR 8705.4, the system developer should submit qualification test plan (QTP) data, or any applicable heritage data, to establish the board level qualification.

b. For mission classes A, B, or C per GPR 8705.4, the system developer shall prepare a QTP and any applicable heritage data to establish the board level qualification.

The GSFC project may choose to review applicable heritage data, including documented technical justification (e.g., test data, rationale, and/or data to support prior successful test campaigns) from the supplier in lieu of reviewing a QTP.

Table 1 – Assembly Qualification Test Guidelines

Test [1]	**Conditions**
Visual Inspection	The interconnects on the test board should have met all visual and radiographic inspection criteria as defined in Sections 4.6.5, Post Soldering Inspection, and 4.6.8, Inspection Points (refer to Table 2, Inspection Requirements Summary)
Electrical Baseline	Electrical continuity testing should be performed to baseline a known good pre-test condition.
Vibration Variable	GSFC-STD-7000, General Environmental Verification Standard (GEVS) for GSFC Flight Programs and Projects
Electrical Continuity [2]	Perform electrical continuity testing of the daisy chained connections at -55°C, +100°C, and 25°C to identify a failed attachment.
Thermal Cycling with Continuous Electrical Monitoring	Per IPC-9701, Paragraph 4.3 and Table 4-1, preconditioning applies. Refer to IPC-9701 for guidance on calculating the acceleration factor, temperature range, and cycle count. These parameters will vary for each mission environment. See IPC-9701 Table 4-4 for electrical

	failure definitions. Thermocouple monitoring of the package, the board, and the test chamber, is recommended.
Cross-Section	At least one area array package should be cross-sectioned through an edge and center row. Buried vias and vias-in-land shall be examined in cross-section.

Note 1: Tests listed are recommended guidelines. Test plans and criteria may be tailored by the project to formulate requirements.

Note 2: Extreme temperatures for electrical tests are chosen to facilitate detection of cracks.

4.6 Manufacturing Process Parameters

4.6.1 Solder Paste Placement

Solder volume shall be determined through engineering process development and shall be a process/quality control parameter to result in uniform interconnect wetting and solder fillets. Visual inspection of the deposited paste shall be performed on 100% of the area array lands. Inspection should verify uniformity, land coverage, and check for misplaced solder.

4.6.2 Part Placement (into the solder, prior to reflow)

Area array packages shall be visually verified to ensure part placement and polarity. Alternate methods for assuring accurate placement of area array parts prior to solder reflow shall be reviewed by MRB and approved by the GSFC project.

4.6.3 Reflow Profile

A development board with a thermal capacity comparable to the flight unit shall be used to develop an appropriate reflow profile. A mechanically representative area array package should be used to determine the thermal profile. The inspection criteria of Section 4.6.8, Inspection Points, shall be used to verify the profile design. See Section **Error! Reference source not found.**, Assembly Process Control Review.

A method for developing a temperature profile and verifying the profile shall be performed using a method that validates that the time/temperature envelope of the reflow system is maintained within an acceptable margin. Temperature data shall be recorded at regular intervals during the reflow process and retained per the record retention requirements of the Project. See IPC-7530 - Guidelines for Temperature Profiling for Mass Soldering Processes (Reflow and Wave). For part removal and replacement, see 4.8.

4.6.4 Post-Soldering Cleaning

Cleaning requirements shall be in accordance with NASA-STD-8739.6.

4.6.5 Post-Soldering Inspection

The inspection of the area array solder joints shall meet all applicable requirements of IPC J-STD-001 Space Addendum and the following:

4.6.5.1 Visual Inspection of Outer Row Solder Joints

Visual inspection of all outer row area array solder joints (top and bottom) shall be performed per IPC J-STD-001. Inner row solder joints should also be inspected to the greatest extent, if possible, to IPC J-STD-001.

4.6.5.2 Radiographic Inspection (X-ray)

All area array interconnects shall be inspected using radiographic methods to screen for workmanship defects. X-ray equipment shall allow the operator to view the assembled PWA in an

oblique view, such that each individual interconnect can be inspected, including the solder joints at the part and board sides (refer to Figure 1). Non-conformances to the criteria of IPC J-STD-001 Space Addendum shall require MRB approval.

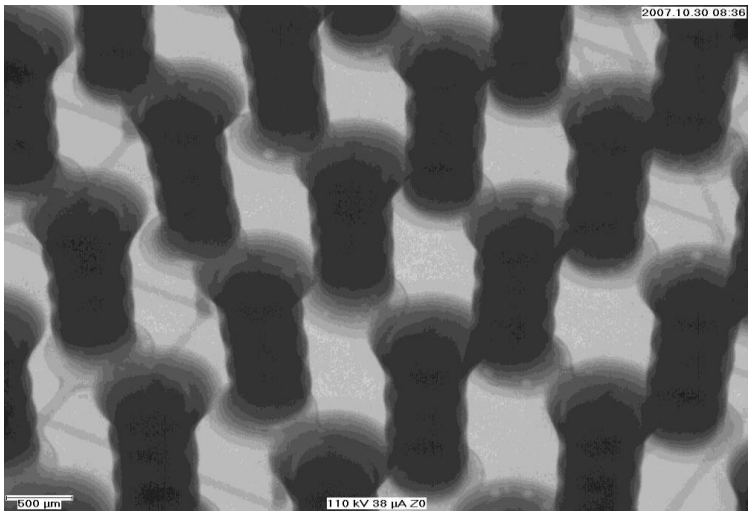

Figure 1- Example of an Oblique X-ray view showing an Acceptable level of voiding in the solder joints.

4.6.6 Staking

Staking shall not contact solder joints or any of the interconnects. Staking shall meet all applicable quality requirements of NASA-STD-8739.1.

4.6.7 Conformal Coating

Conformal coating of boards with area array packages shall follow the requirements of IPC-7095 and NASA-STD-8739.1.

4.6.8 Inspection Points

A summary of the recommended inspection requirements is provided in Table 2.

Table 2- Inspection Requirements Summary

Inspection Point and Inspection	Section Reference
Area Array Package Incoming Inspection As-received part	4.2.3
PWB Incoming Inspection Solder Mask Inspection Board Flatness Area Array Land Inspection Area Array Land Pattern Flatness	 4.2.4.1 4.2.4.2 4.2.4.3 4.2.4.4
Soldering Preparation Solder paste volume and placement	4.6.1
Part placement	4.6.2
Workmanship Inspection, soldering, solder joints	4.6.5

Workmanship	4.6.6
Inspection, polymeric applications, staking and conformal coating	4.6.7

4.7 **Assembly Process Control Review**

The GSFC Project and QA shall review and approve the supplier's soldering assembly process prior to manufacture of flight boards.

Data generated as a result of supplier's soldering assembly process development/validation may be requested for review by the GSFC Project. Additional soldering process validation testing may be required to demonstrate that the supplier's method of attachment is capable of meeting the requirements herein.

4.8 **Part Removal and Replacement**

Part removal and replacement processes shall be documented. Repairs and rework require prior review and approval in accordance with the GSFC Project's Approved Anomaly Reporting process prior to implementation. This document does not provide explicit guidance on the maximum number of rework/repair cycles a PCB may be subject to. The GSFC Project, through an MRB, will review and approve the documentation for part removal and replacement, inspection, and reflow profile prior to carrying out rework procedures to verify the supplier's ability to rework area array packages using a process which minimizes part or board damage. See Section 4.5 for assembly qualification testing requirements. Interconnects shall not be reused even if they remain attached to the part after part removal from the board and appear acceptable. The area array region of the board, at a minimum, shall be visually inspected and results recorded for any instances of damage, solder mask damage, land/trace damage, board warpage, and cleanliness, after area array package removal and land redressing, prior to the installation of a new part. Placement of newly applied solder paste shall also be inspected prior to the installation of a new part. In addition, the newly placed replacement part shall be inspected for proper placement and polarity prior to the reflow operation. Final inspection of the reflowed area array package shall be in accordance with Section 4.6.5, Post-Soldering Inspection.

APPENDIX A.

SUGGESTED READING

The following works include reliability and design aspects that have driven the development of the requirements herein. These works are non-inclusive to the requirements herein and are supplementary in nature.

1. Suh, Jong-ook. Virtex-5 CN package daisy chain evaluation test report. Pasadena, CA: Jet Propulsion Laboratory, National Aeronautics and Space Administration, 2016, 2016. https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20170008013.pdf
2. Ghaffarian, Reza. Reliability of CGA/LGA/HDI Package Board/Assembly. Pasadena, CA: Jet Propulsion Laboratory, National Aeronautics and Space Administration, 2012, 2012. https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20160001775.pdf
3. Fleisher, Jonathan, and Walter Willing. "Study of Column Grid Array components for space systems." Reliability and Maintainability Symposium (RAMS), 2012 Proceedings-Annual. IEEE, 2012. http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=6175511
4. Mehta, Atul C., and Charles C. Bodie. "Column grid array rework for high reliability." (2008). https://trs.jpl.nasa.gov/bitstream/handle/2014/41579/08-4771.pdf?sequence=1
5. Ghaffarian, Reza. "Thermal cycle reliability and failure mechanisms of CCGA and PBGA assemblies with and without corner staking." IEEE Transactions on Components and Packaging Technologies 31.2 (2008): 285-296. http://ieeexplore.ieee.org/document/4520013/